TECHNOLOGY LEADERSHIP

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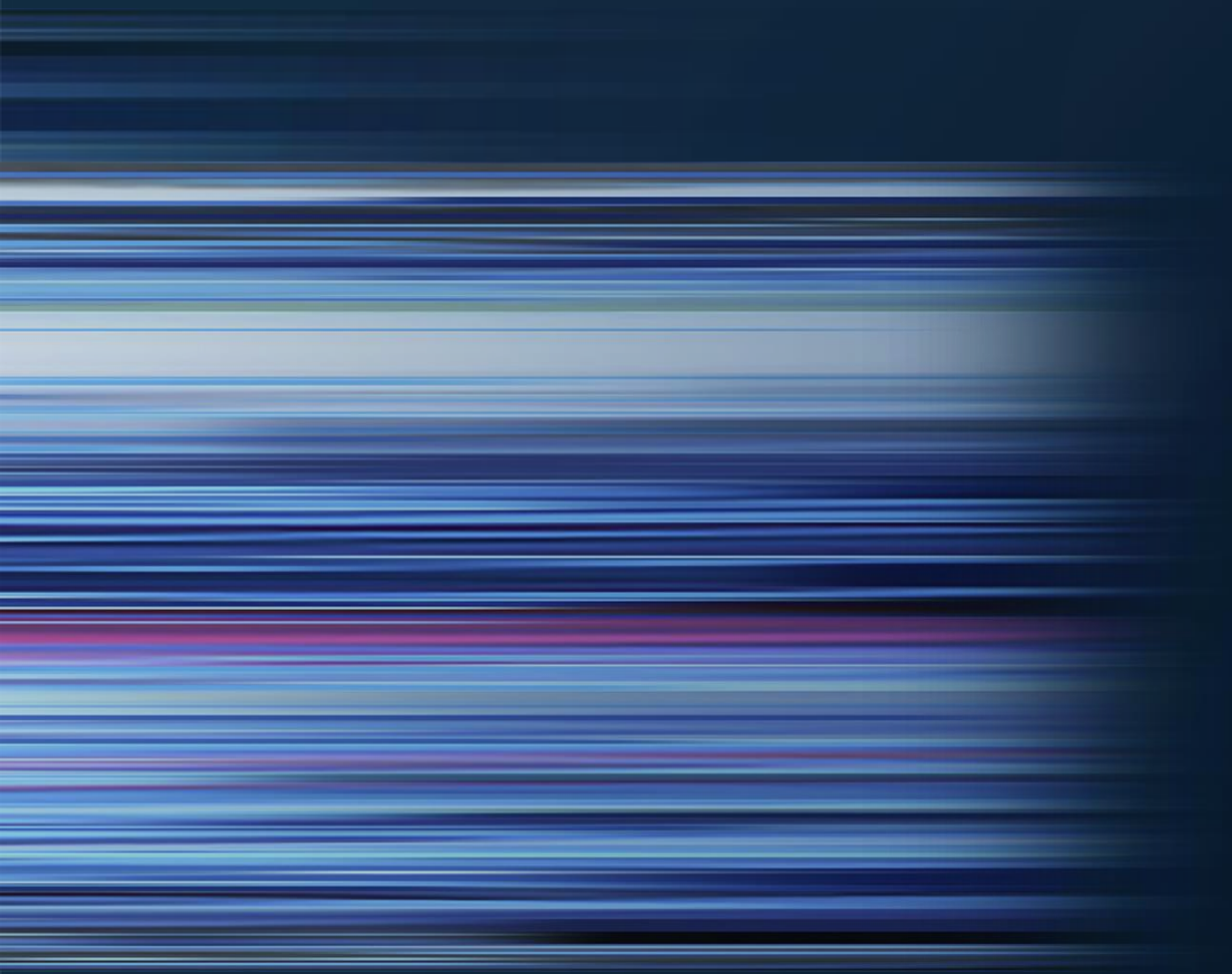
LEGAL DISCLAIMER

DISCLOSURES

China Tech and Manufacturing Day 2017 occurs during Intel's "Quiet Period," before Intel announces its 2017 third quarter financial and operating results. Therefore, presenters will not be addressing third quarter information during this year's program.

Statements in this presentation that refer to forecasts, future plans and expectations are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "continues," "may," "will," "would," "should," "could," and variations of such words and similar expressions are intended to identify such forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Such statements are based on management's expectations as of September 19-20, 2017, and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations are set forth in Intel's earnings release dated July 27, 2017, which is included as an exhibit to Intel's Form 8-K furnished to the SEC on such date. Additional information regarding these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent reports on Forms 10-K, 10-Q and 8-K reports may be obtained by visiting our Investor Relations website at www.intc.com or the SEC's website at www.sec.gov.

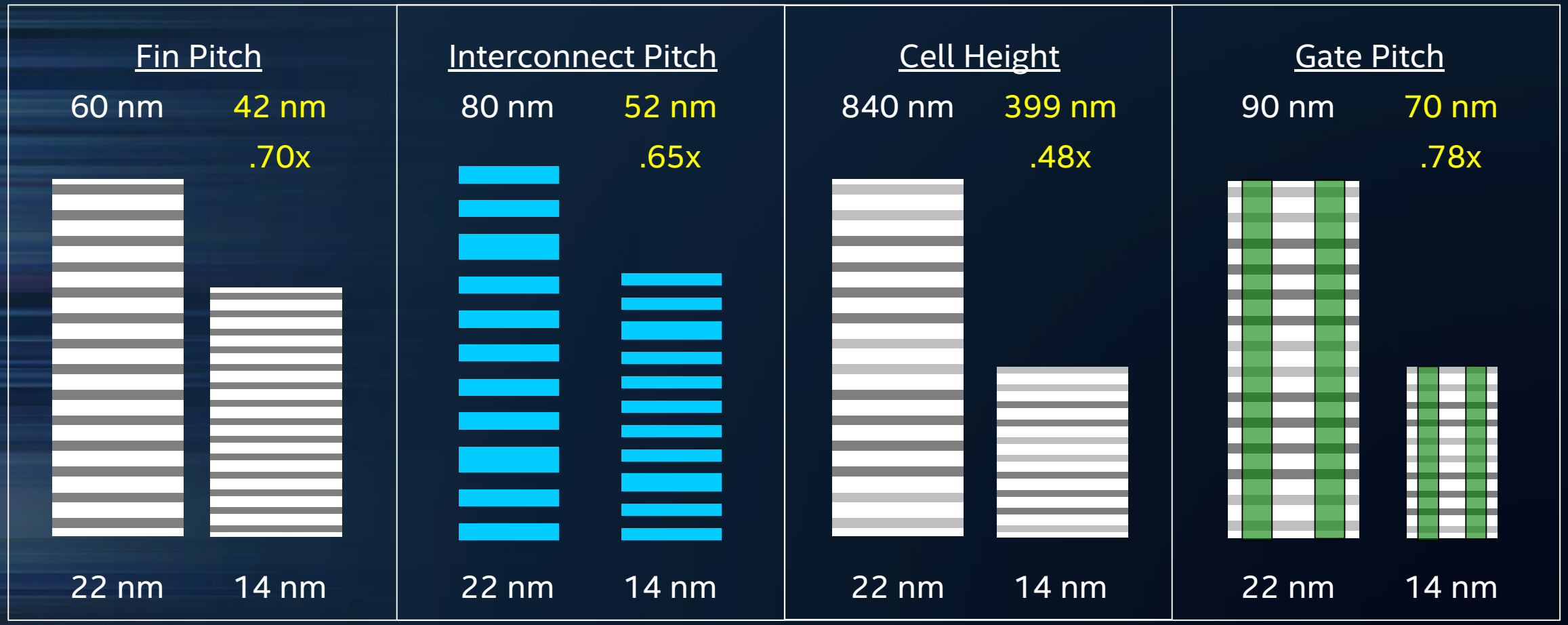


10 NM HYPER SCALING

22FFL TECHNOLOGY

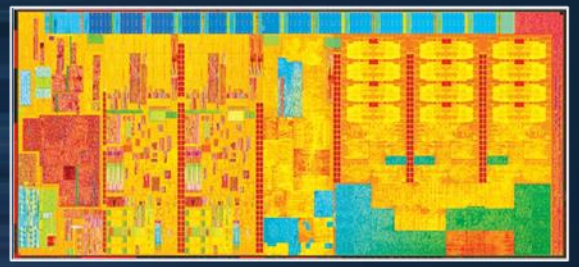
FUTURE RESEARCH

14 NM HYPER SCALING FEATURES



14 nm uses aggressive feature scaling to deliver unprecedented 0.37x logic cell area scaling

14 NM PRODUCTS



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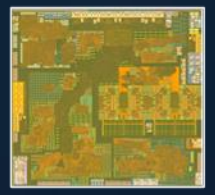

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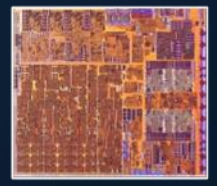

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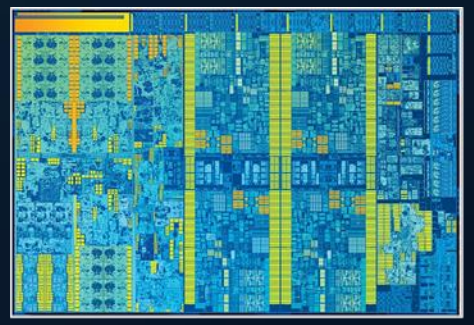

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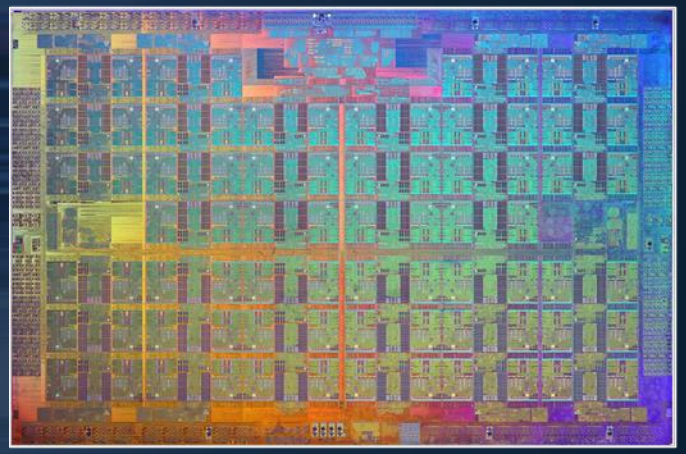

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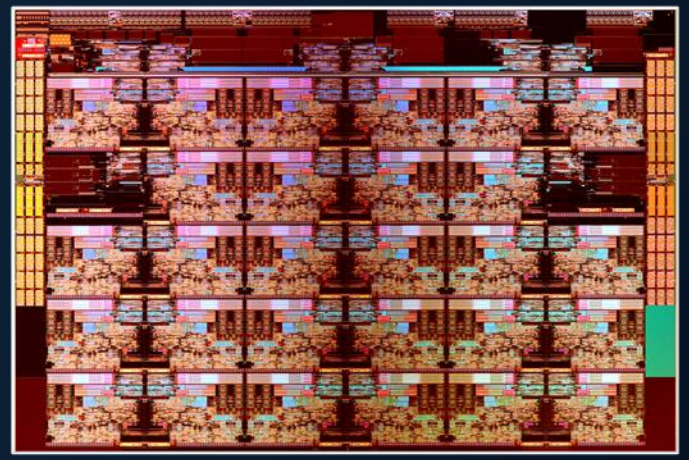

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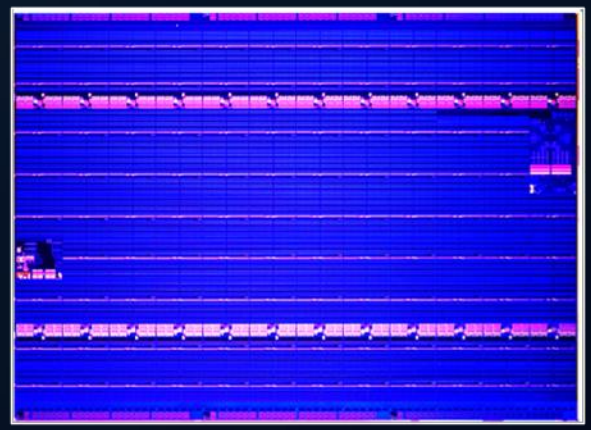
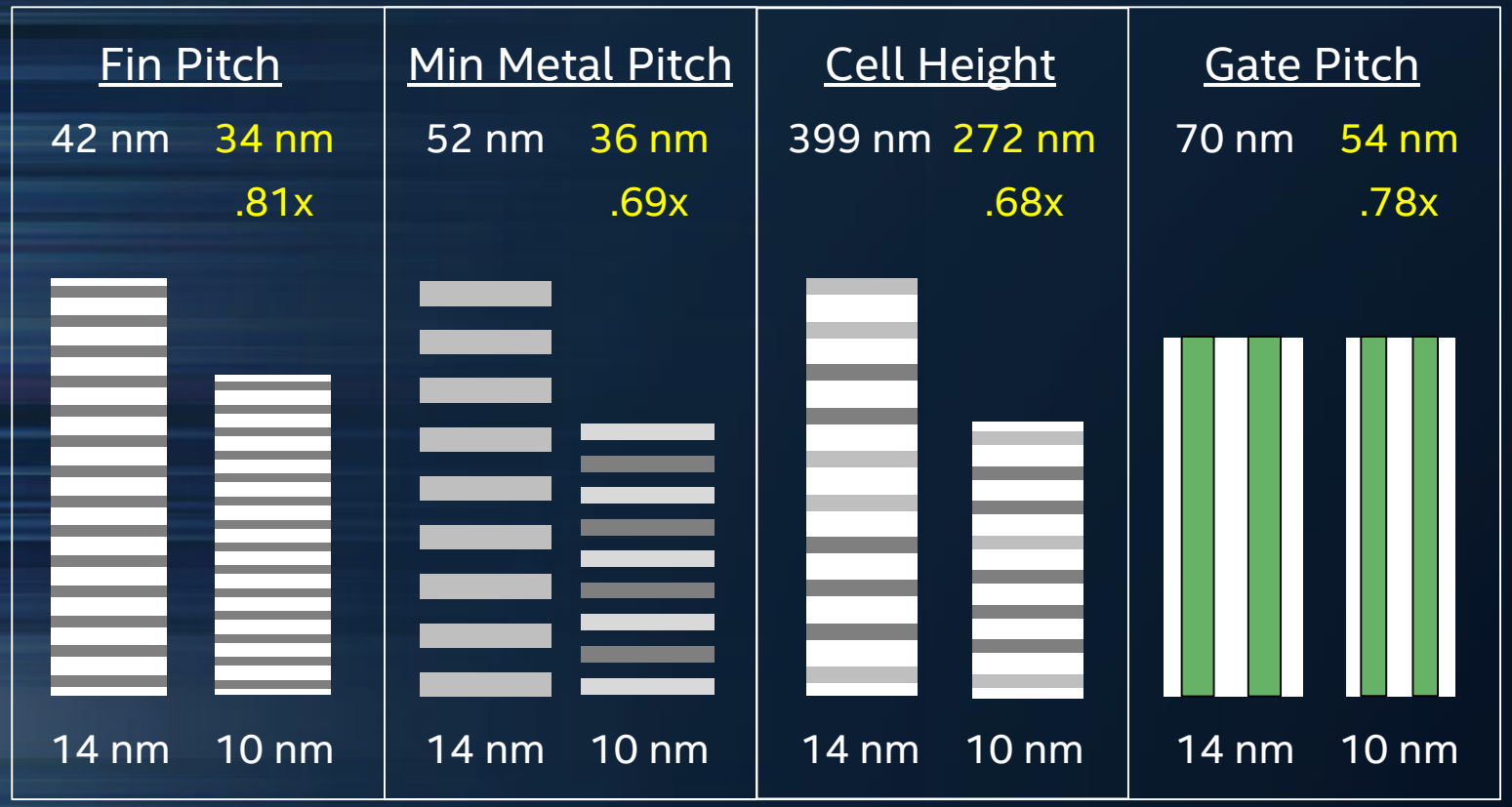


FPGA

Wide range of 14 nm products in volume production on various derivative technologies

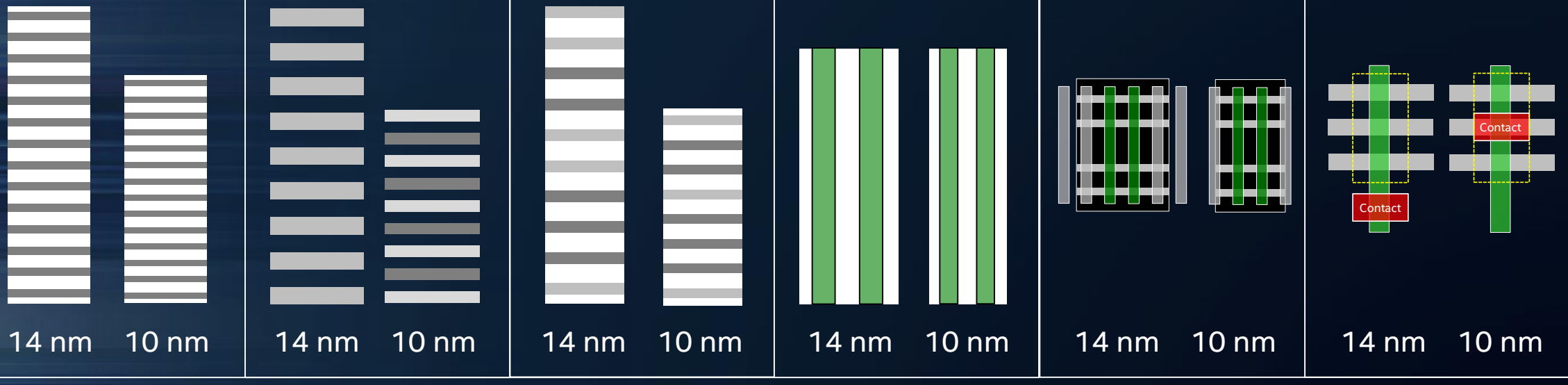
10 NM HYPER SCALING



10 nm features aggressive pitch scaling - world's first self-aligned quad patterning

10 NM HYPER SCALING

Fin Pitch	Min Metal Pitch	Cell Height	Gate Pitch	Dummy Gate	Gate Contact
42 nm → 34 nm (.81x)	52 nm → 36 nm (.69x)	399 nm → 272 nm (.68x)	70 nm → 54 nm (.78x)	Double → Single	Std → COAG
14 nm → 10 nm	14 nm → 10 nm	14 nm → 10 nm	14 nm → 10 nm	14 nm → 10 nm	14 nm → 10 nm

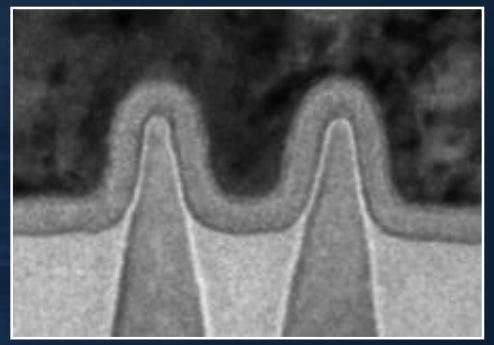


Double Pattern → Quad Pattern

Aggressive scaling & new features deliver 2.7x transistor density improvement

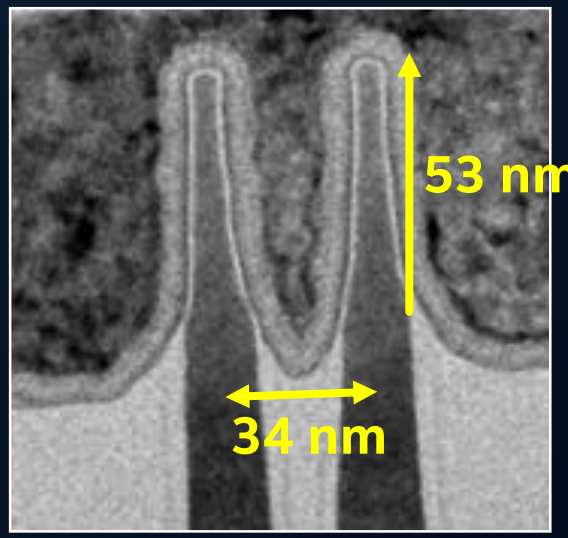
3RD GENERATION FINFETS

22 NM



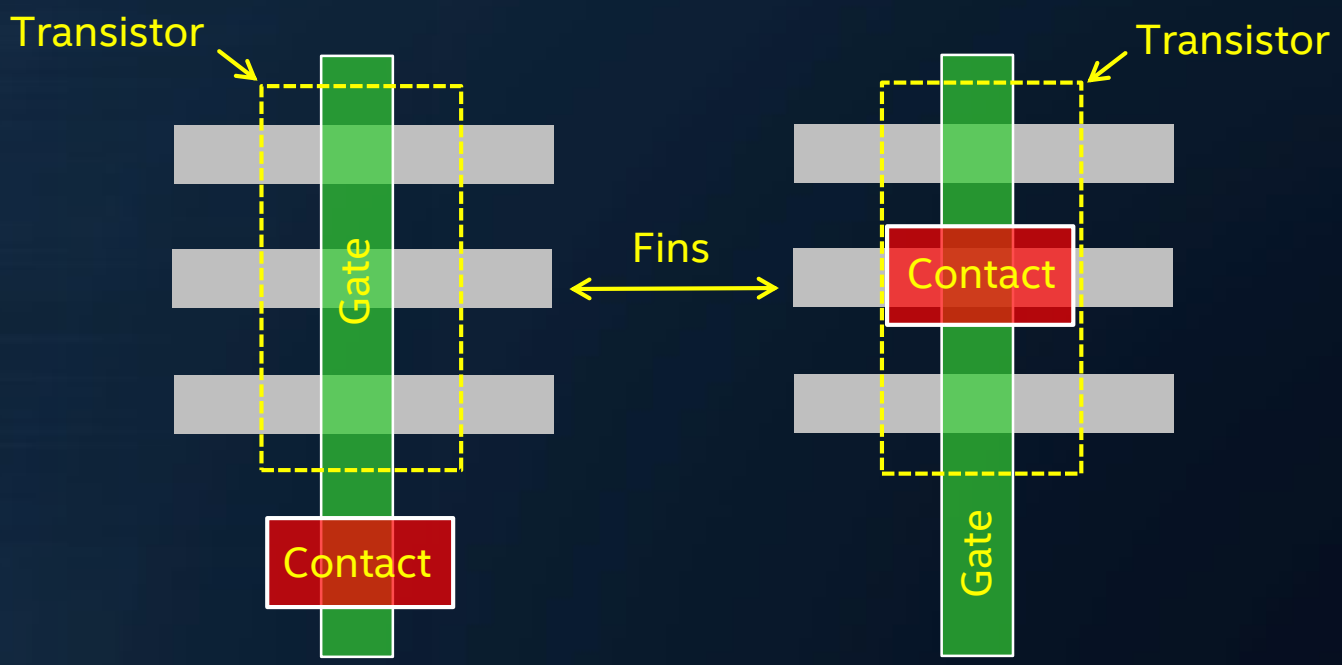
14 NM

10 NM



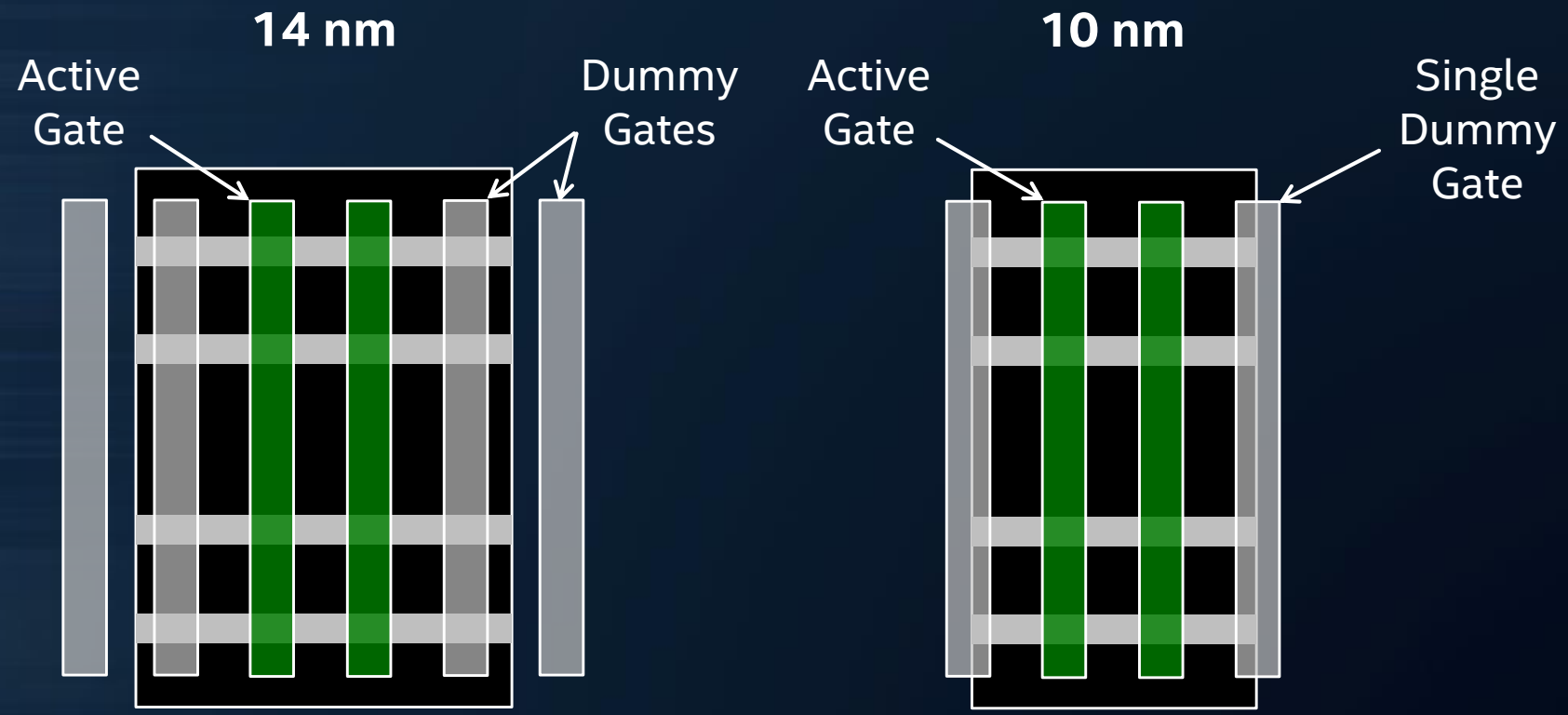
10 nm fins are ~25% taller and ~25% more closely spaced than 14 nm

CONTACT OVER ACTIVE GATE



Contact over active gate is a revolutionary feature for another ~10% area scaling

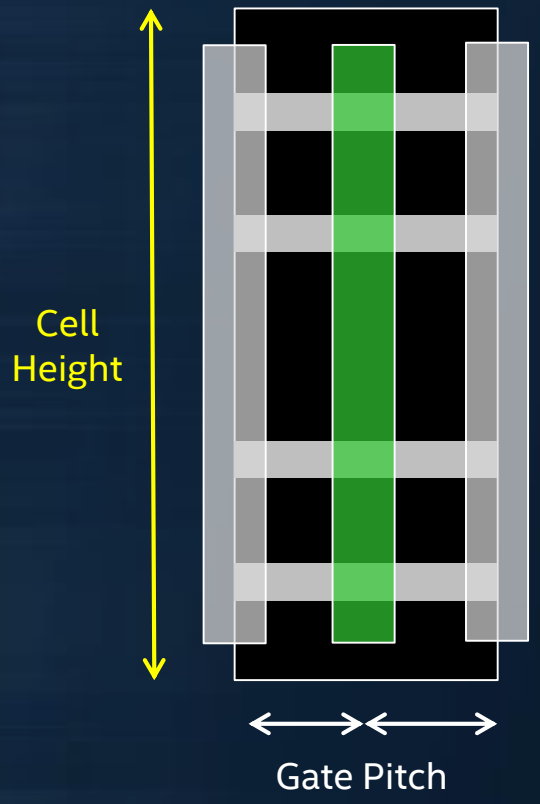
SINGLE DUMMY GATE



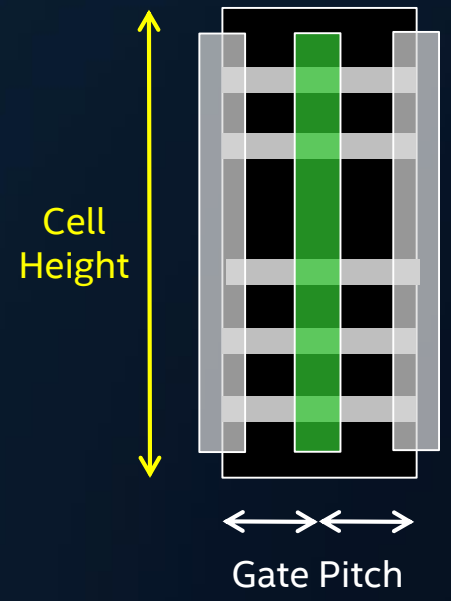
Process innovations enable denser single dummy gate at cell borders

CELL LIBRARY HEIGHT SCALING

14 nm
399nm Height

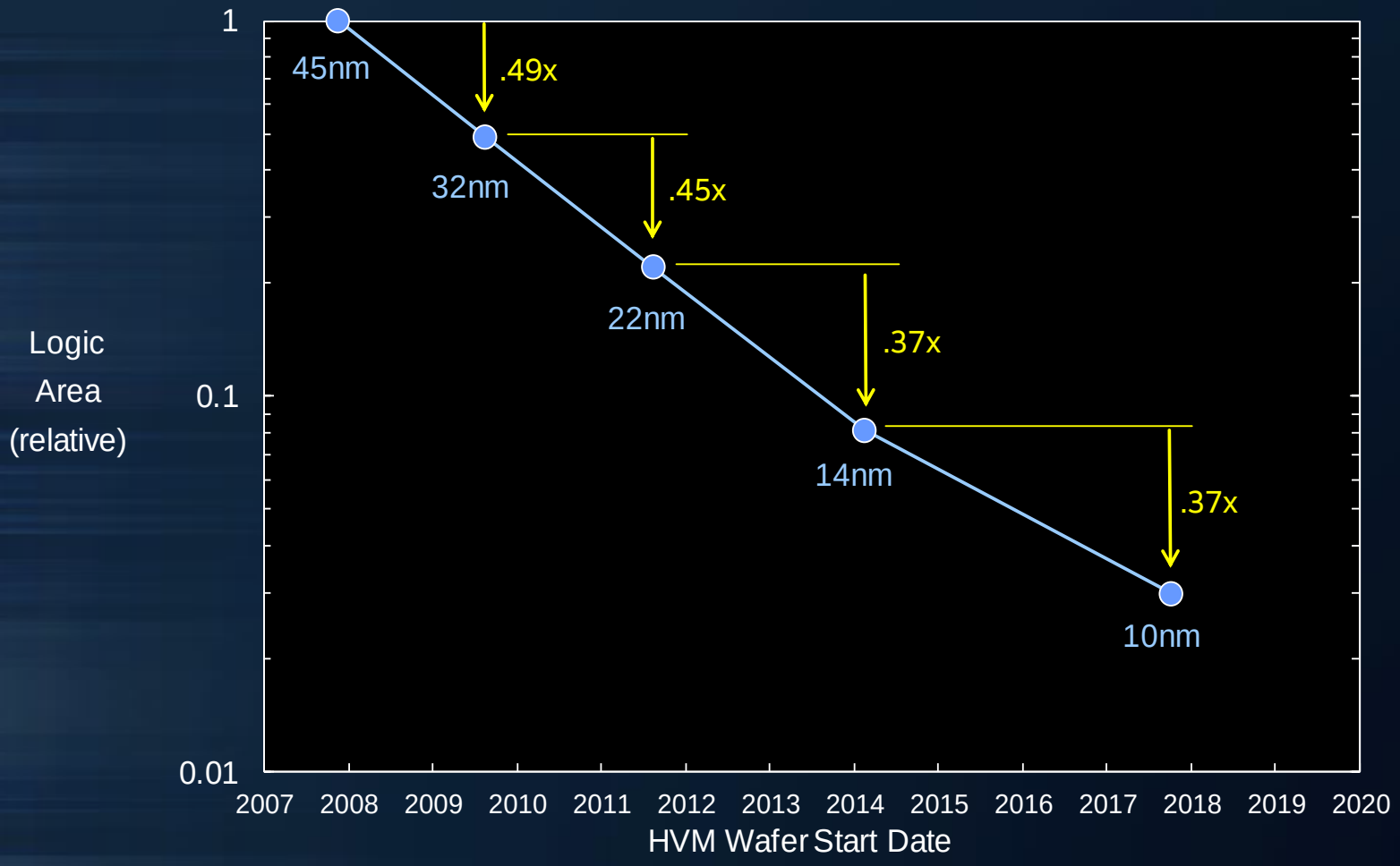


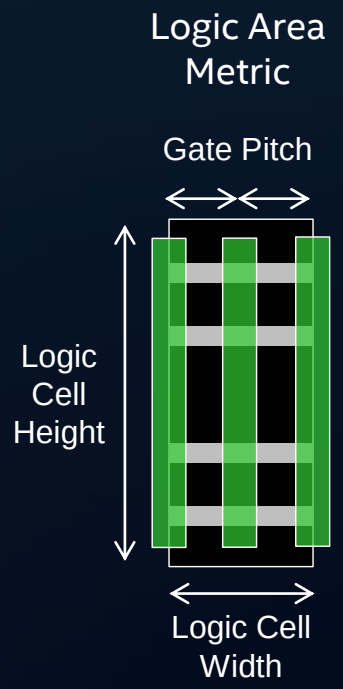
10 nm
272nm Height
(0.68x)



Fin pitch and metal pitch scaling allow cell height to scale 0.68x from 14 nm

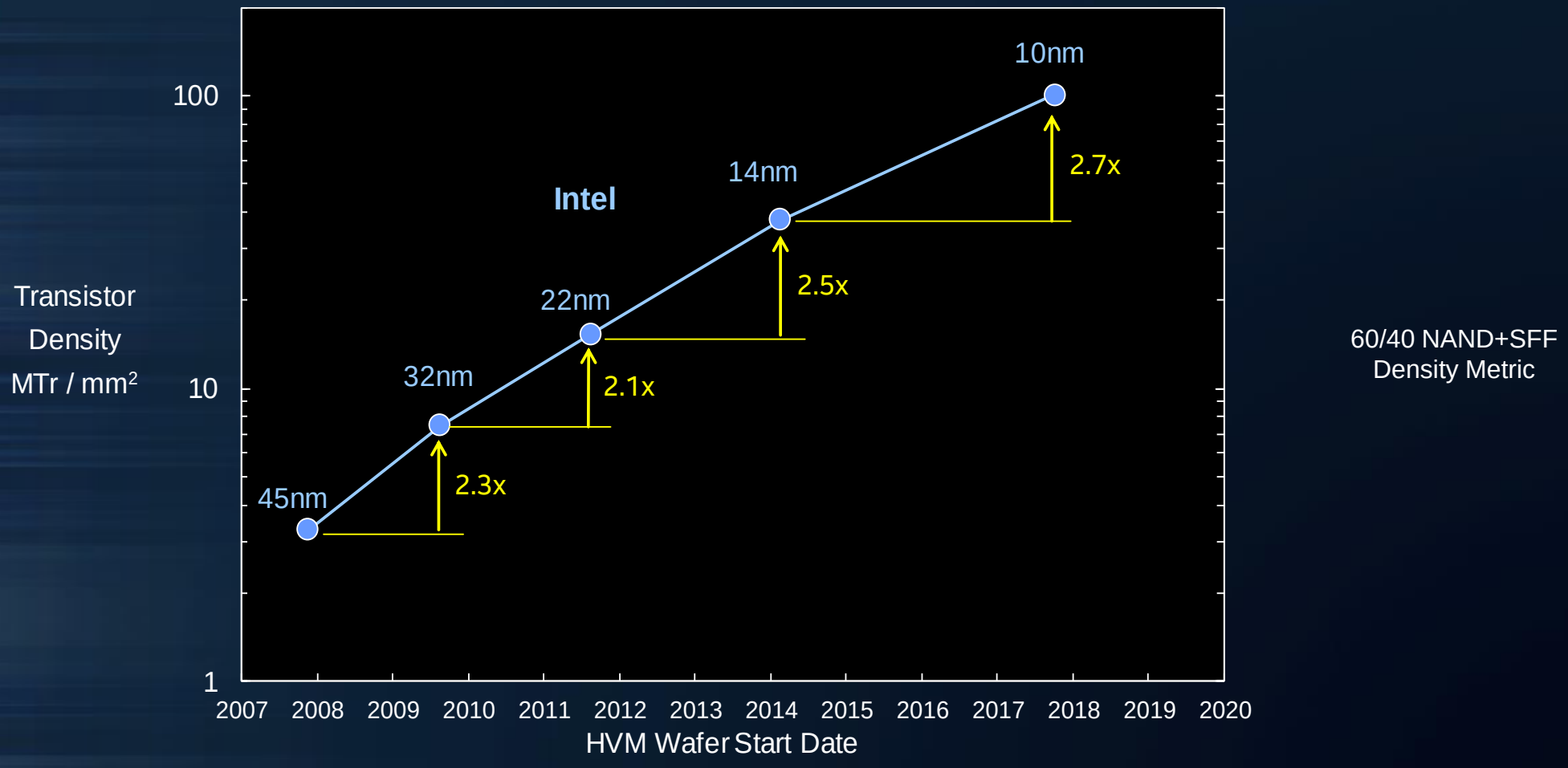
LOGIC TRANSISTOR DENSITY





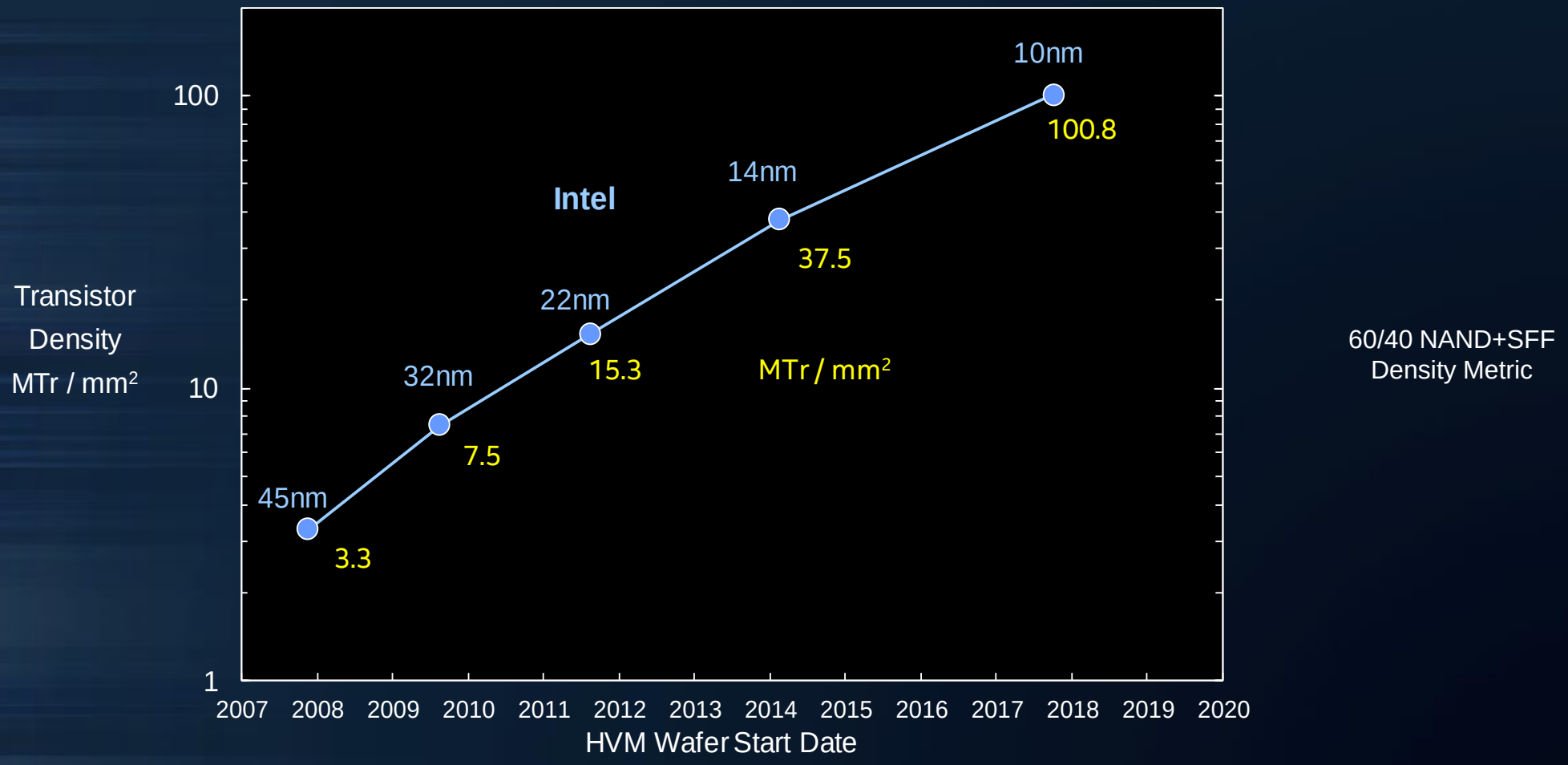
Hyper scaling delivers better-than-normal logic area scaling

LOGIC TRANSISTOR DENSITY



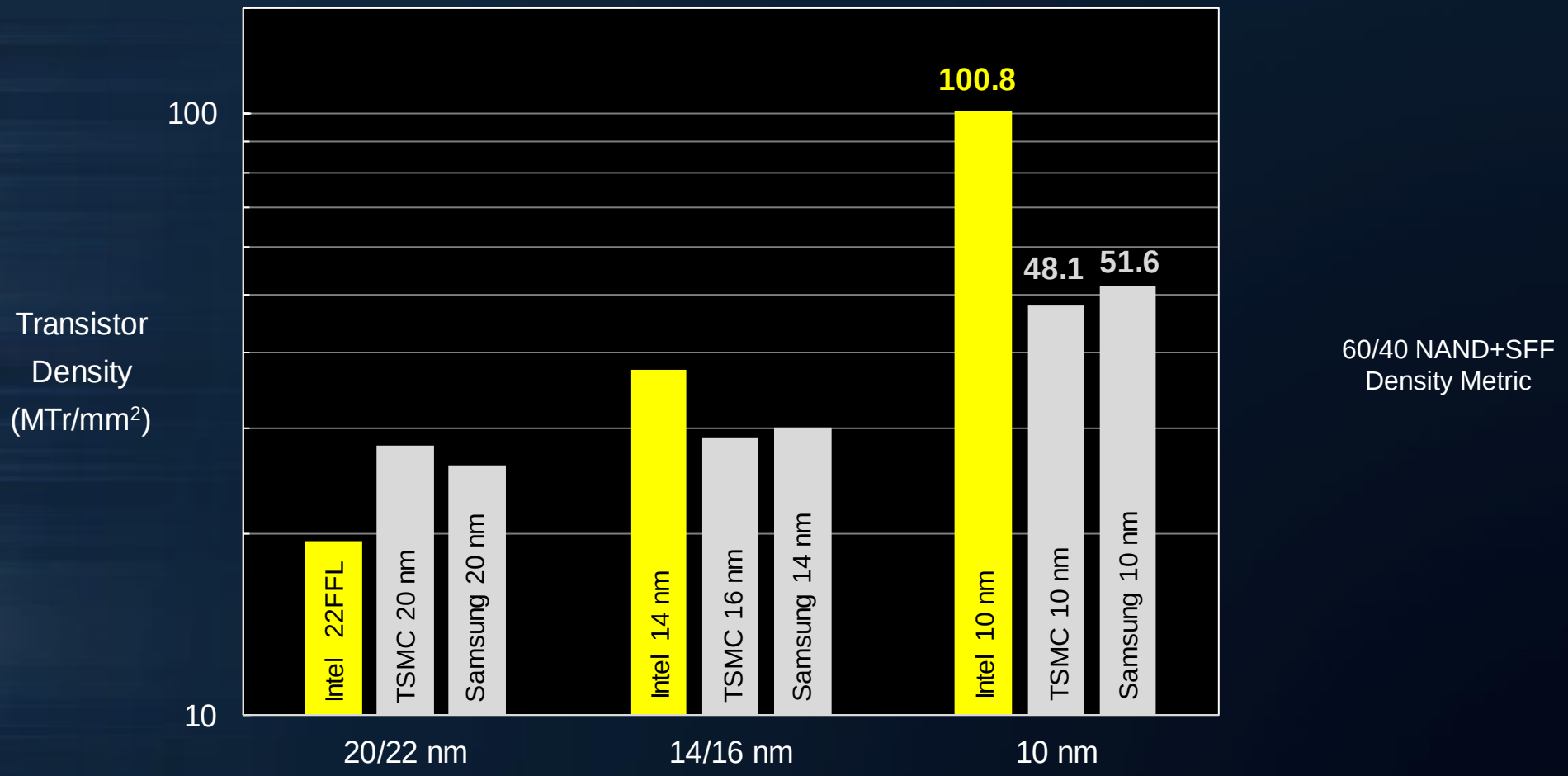
Hyper scaling delivers better-than-normal transistor density improvement

LOGIC TRANSISTOR DENSITY



10 nm hyper scaling features result in transistor density above 100 MTr/mm²

LOGIC TRANSISTOR DENSITY COMPARISON



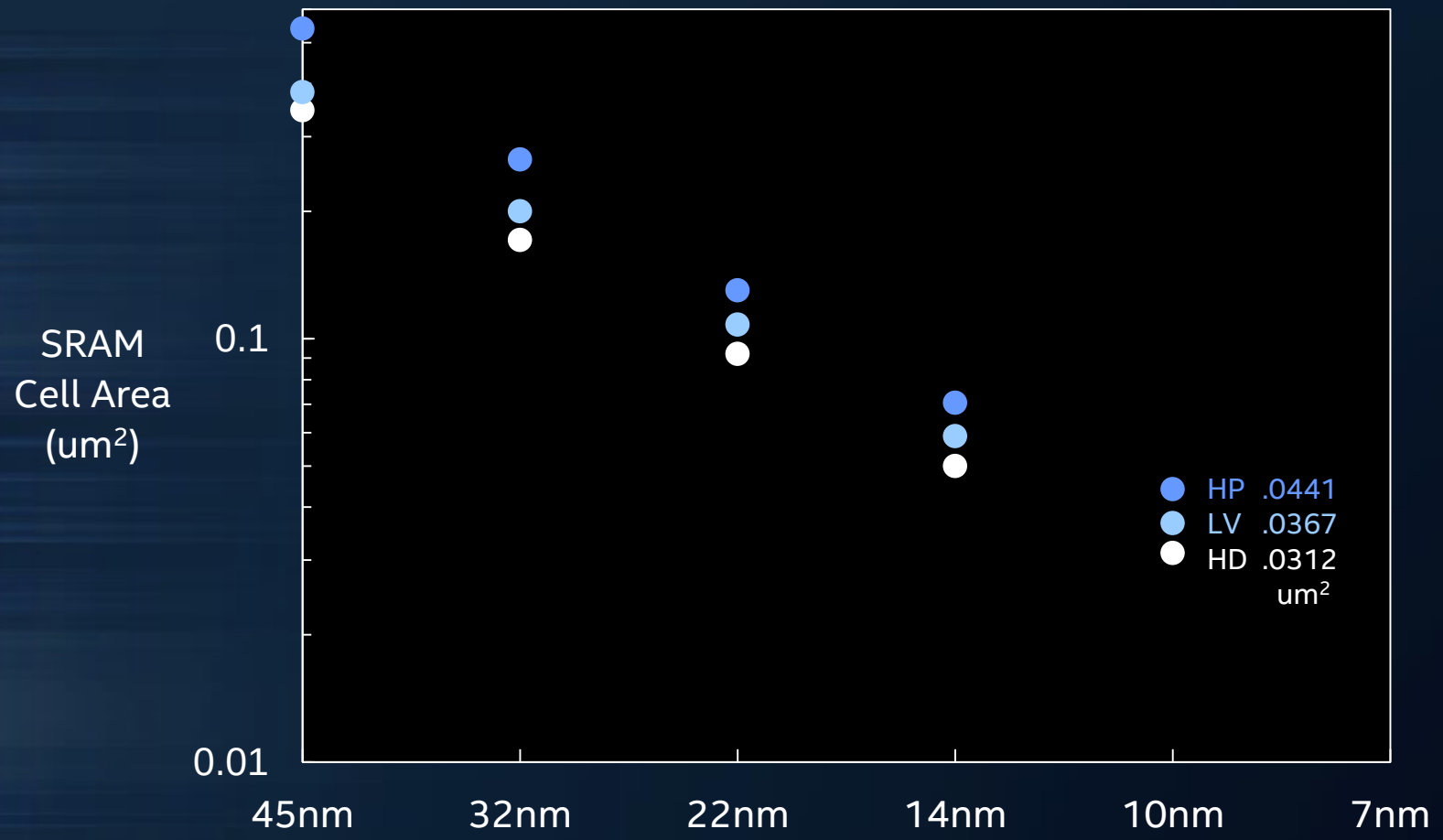
Intel 10 nm is a full generation denser than other “10 nm”

10 NM TECHNOLOGY DENSITY COMPARISON

	Intel 10 nm	TSMC 10 nm	Samsung 10 nm	
Fin Pitch	34	36	42	nm
Gate Pitch	54	66	68	nm
Minimum Metal Pitch	36	42	48	nm
Logic Cell Height	272	360	420	nm
Logic Trans. Density	100.8	48.1	51.6	MTr/mm^2
Logic Trans. Density	1x	0.48x	0.51x	Relative

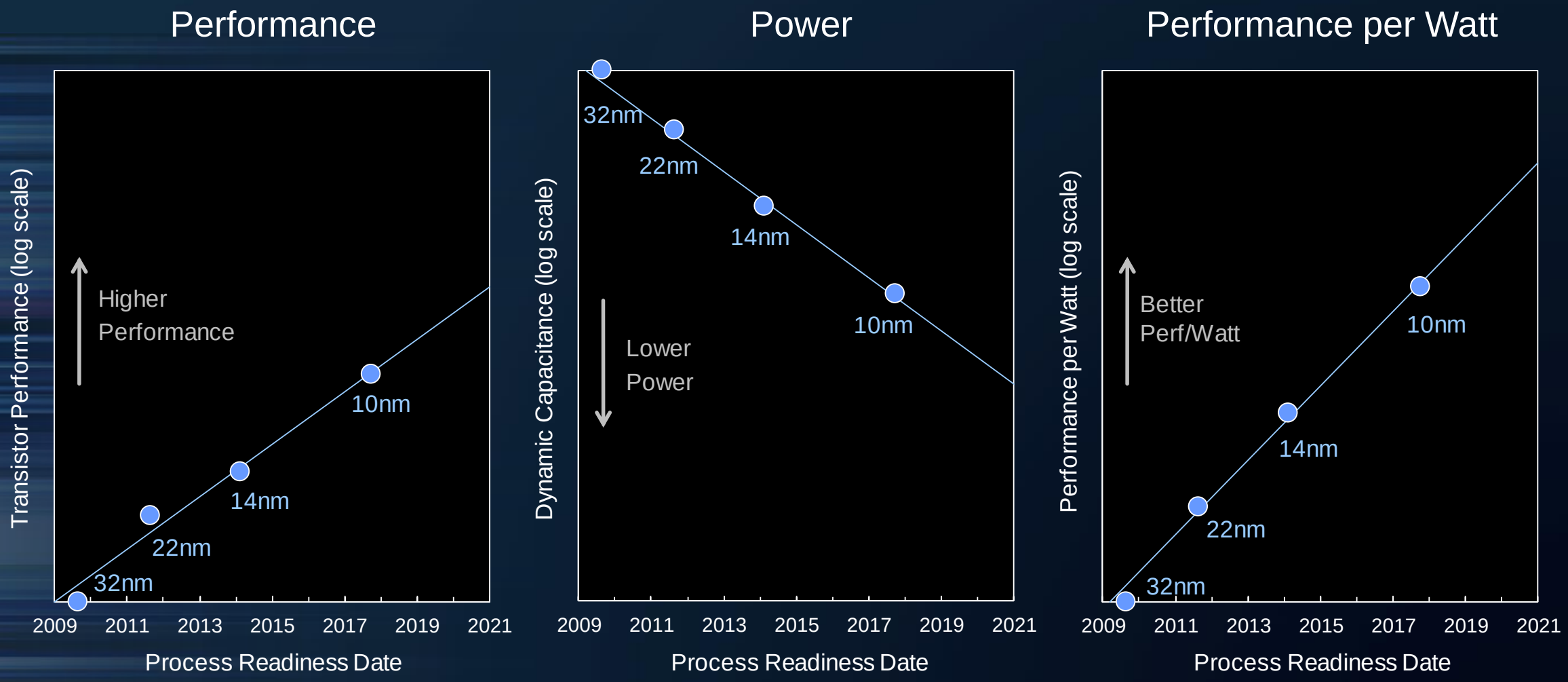
Intel 10 nm is ahead of other “10 nm” technologies on every density metric

SRAM AREA SCALING



10 nm offers a range of SRAM cells for density and power/performance
SRAM cell area scaled ~0.6x from 14 nm

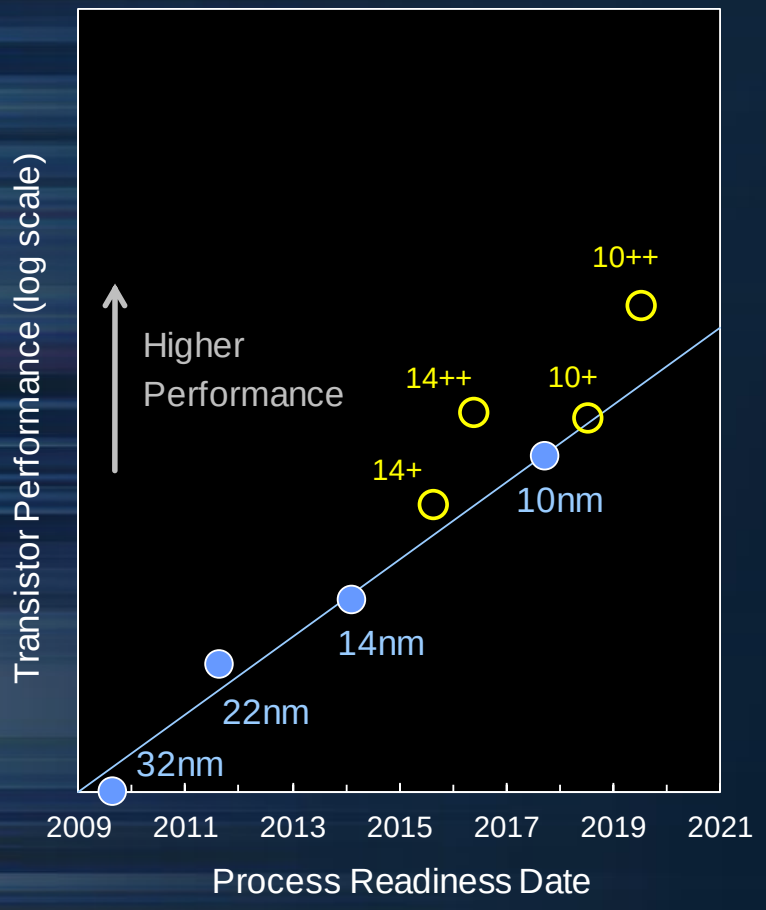
TRANSISTOR PERFORMANCE AND POWER



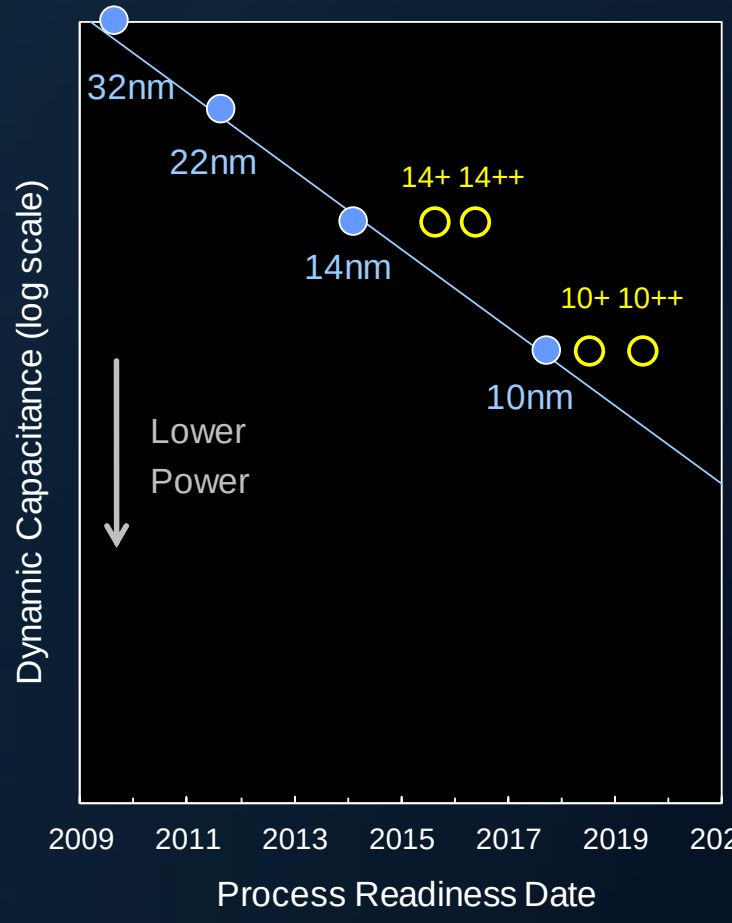
10 nm transistors provide improved performance per watt

TRANSISTOR PERFORMANCE AND POWER

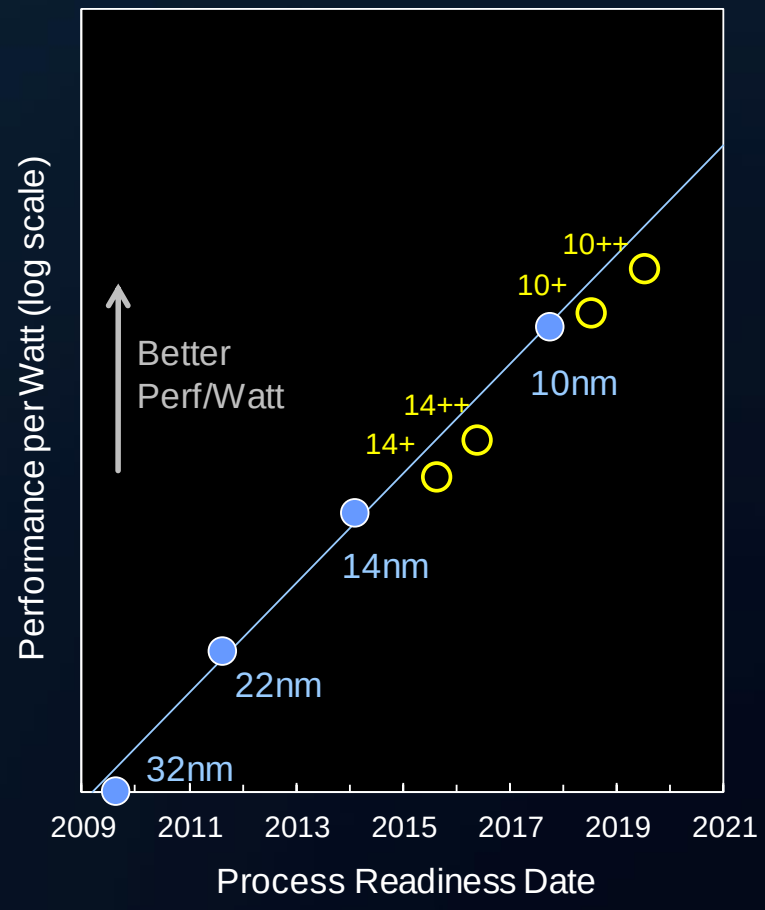
Performance



Power

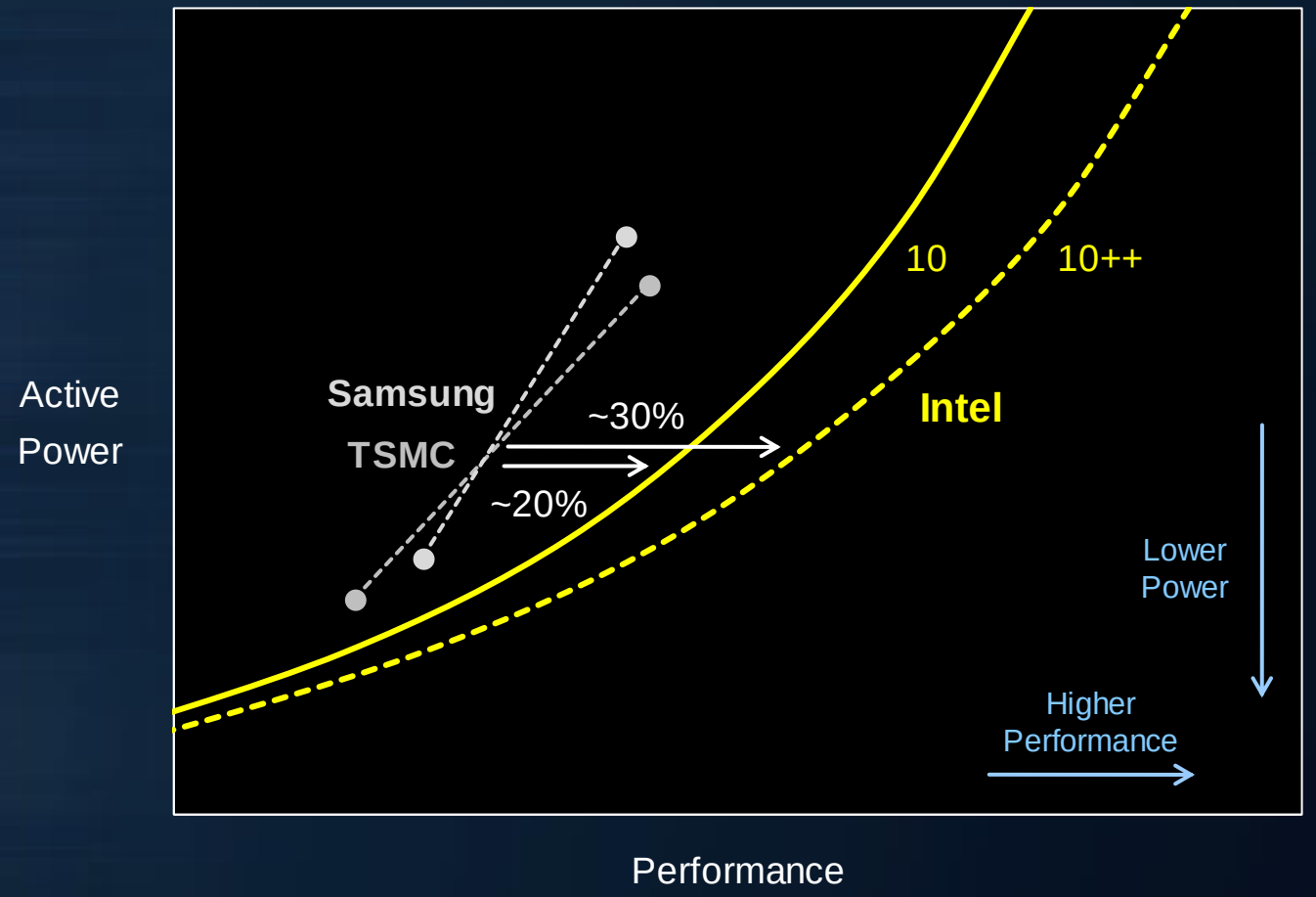


Performance per Watt



10 nm enhancements improve performance and extend technology life

10NM PERFORMANCE AND POWER COMPARISON

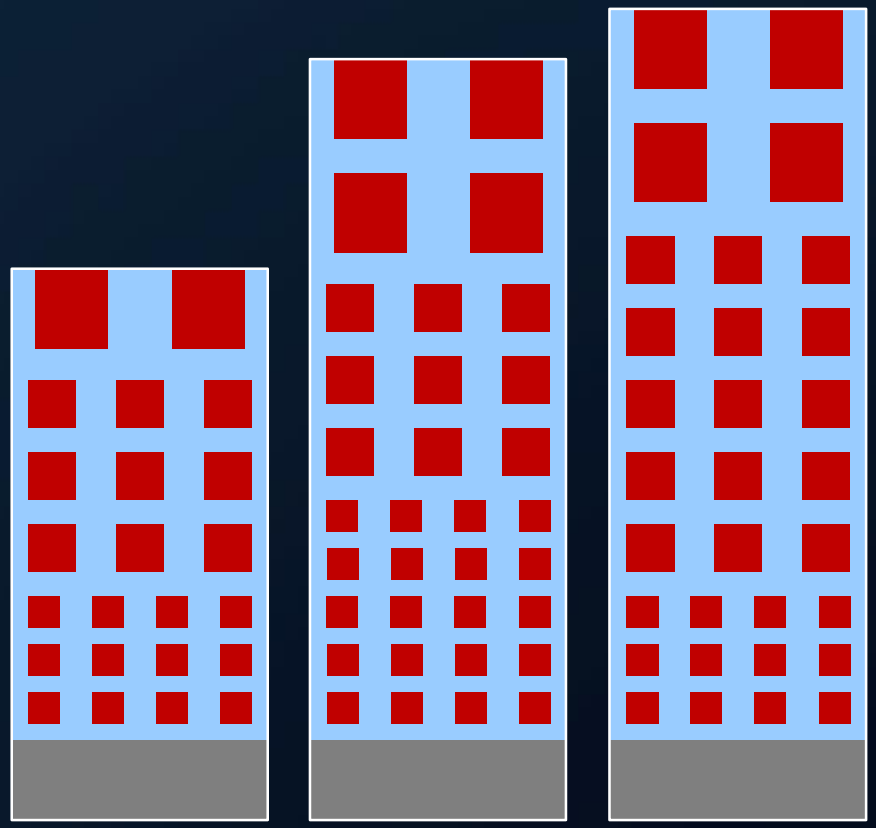


Intel 10 nm has a considerable performance lead over other “10 nm”

DERIVATIVE TECHNOLOGIES

	CPU	SoC
High Perf Transistors	Yes	Yes
Low Leakage Transistors	-	Yes
Analog/RF Transistors	-	Yes
HV I/O Transistors	-	Yes
High-Q Inductors	-	Yes
Precision Resistors	Yes	Yes
MIMCAP	Yes	Yes

Device Options

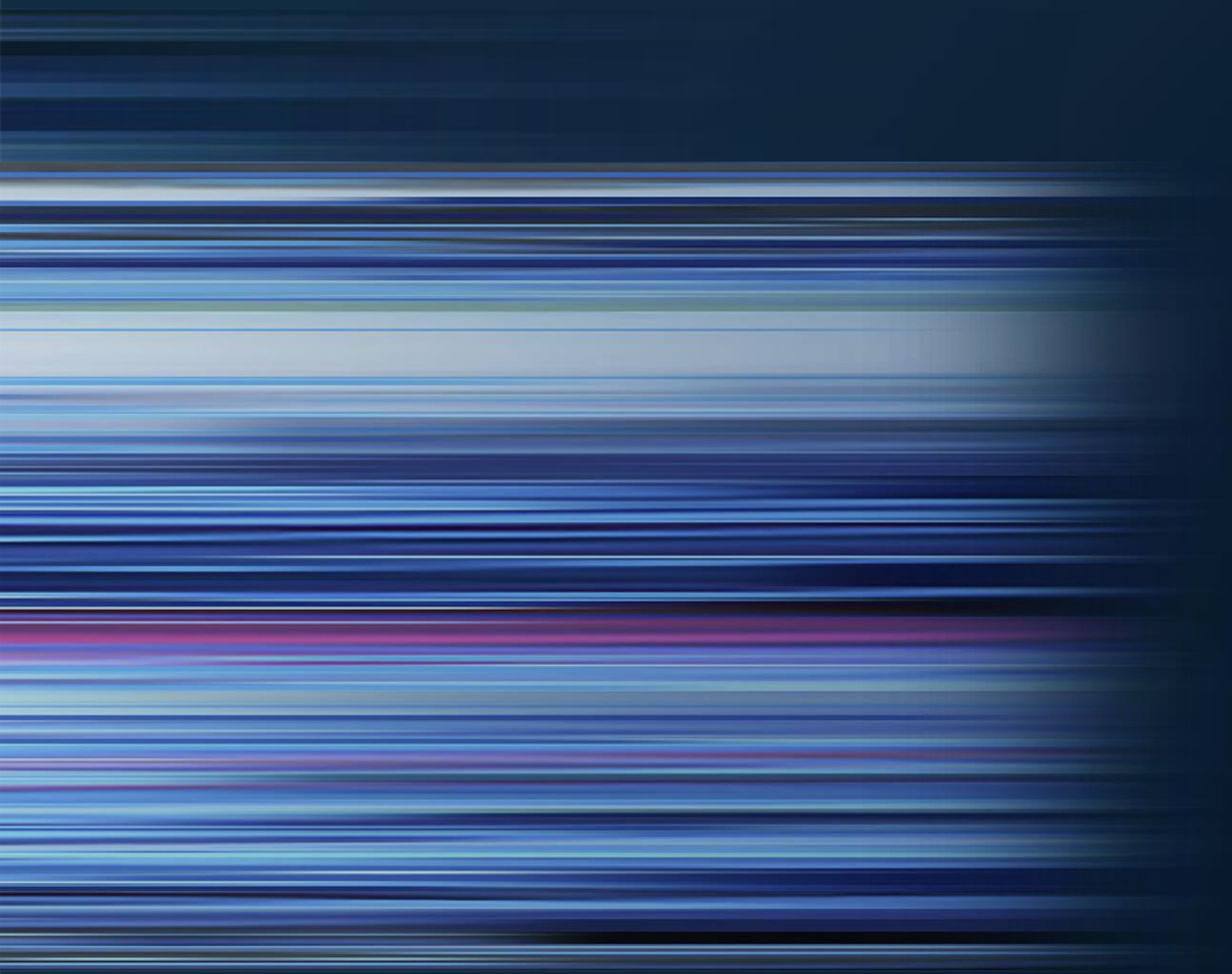


Interconnect Stack Options

Multiple derivative options offered for each technology generation

10 NM SUMMARY

- Intel's 10 nm process technology has the world's tightest transistor & metal pitches along with hyper scaling features for leadership density
- Intel's 10 nm technology is a full generation ahead of other "10 nm" technologies
- Intel's 10 nm process technology is on track to commence manufacturing in 2H'17
- Hyper scaling extracts the full value of multi-patterning schemes and allows Intel to continue the economic benefits of Moore's Law



10 NM HYPER SCALING

22FFL TECHNOLOGY

FUTURE RESEARCH

INTEL'S NEW 22FFL TECHNOLOGY

22FFL is the world's first FinFET technology for low power IOT and mobile products

- Advanced FinFET transistors based on proven 22 nm and 14 nm features
- >100x leakage power reduction with new ultra-low leakage transistor option
- Simplified interconnects and design rules based on 22 nm technology
- New levels of design automation
- Fully RF design enabled
- Cost competitive with other industry 28/22 nm planar technologies

22FFL DIMENSIONS

	22 nm	22FFL	14 nm	
Transistor	FinFET	FinFET	FinFET	
Fin Pitch	60	45	42	nm
Gate Pitch	90	108	70	nm
Metal Pitch	80	90	52	nm
Logic Cell Ht	840	540	399	nm
Trans. Density	15.3	19.4	37.5	MTr / mm^2
SRAM Cell	.092	.088	.050	um^2

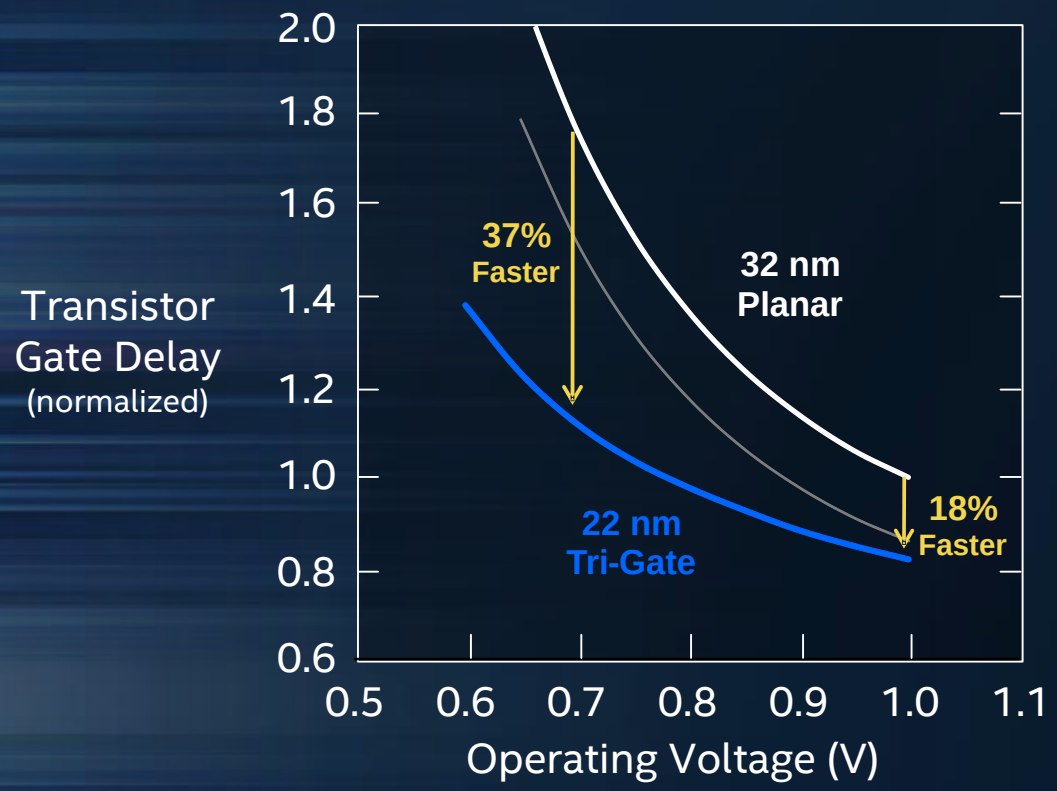
22FFL is based on proven 22 nm and 14 nm features

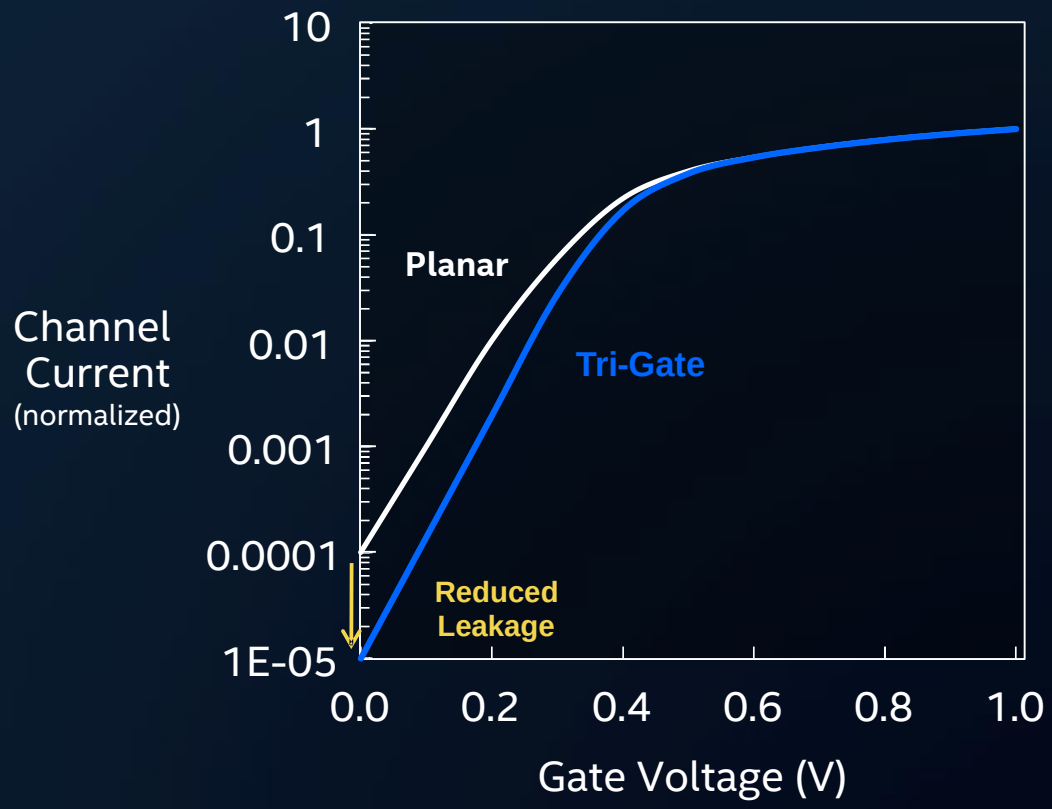
22FFL DEVICES

- ✓ High performance transistors
- ✓ Ultra low leakage transistors
- ✓ Analog transistors
- ✓ High voltage I/O transistors
- ✓ High voltage power transistors
- ✓ Good device matching
- ✓ Low 1/F noise
- ✓ Deep N-well isolation
- ✓ Precision resistor
- ✓ MIM capacitor
- ✓ High resistance substrate
- ✓ High-Q inductors

22FFL offers a wide range of devices for digital and analog/RF design

FINFET PERFORMANCE AND LEAKAGE ADVANTAGE

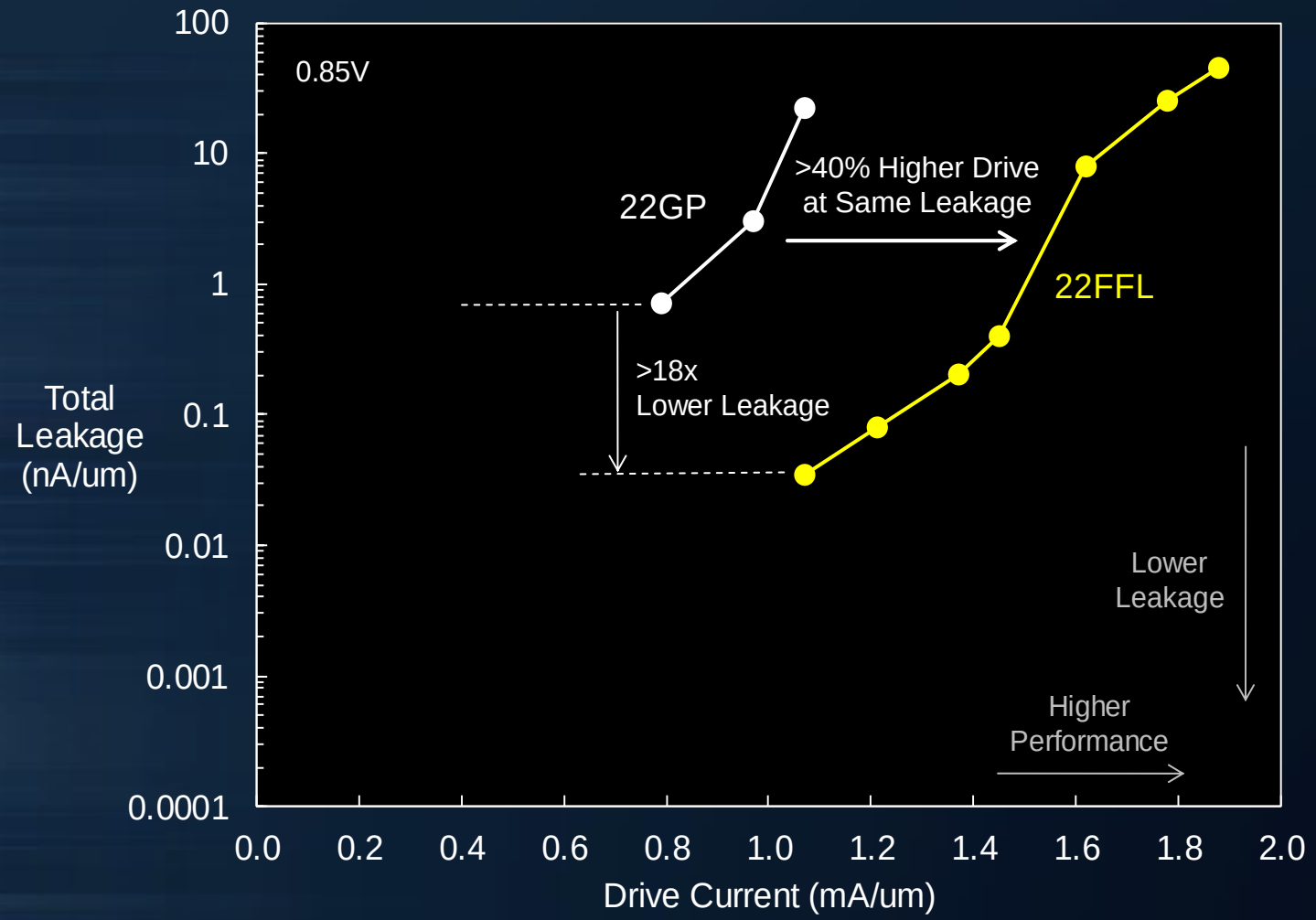




FinFETs provide a significant performance and leakage advantage over any planar transistor

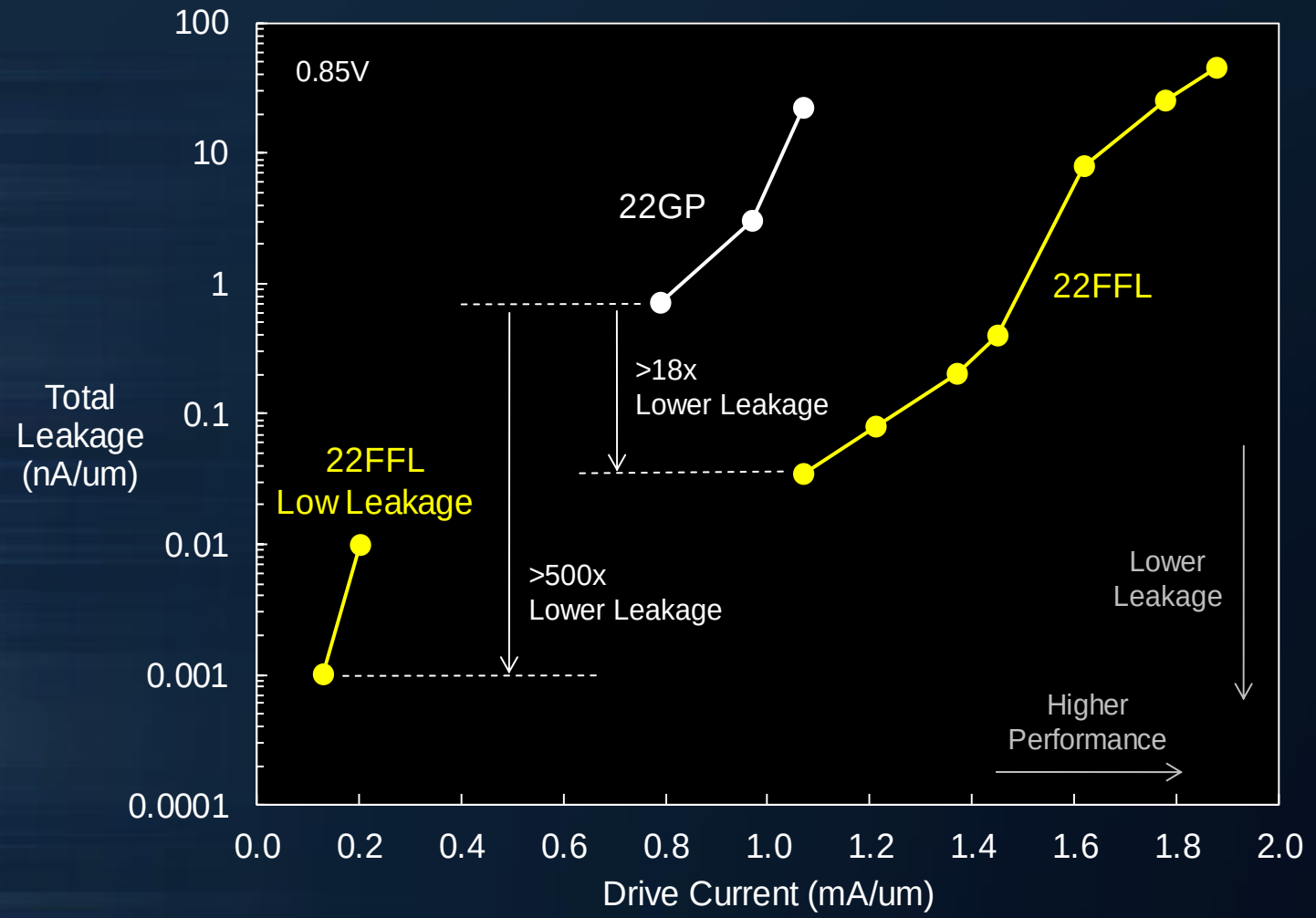
Intel 22 nm Tri-Gate announcement, April 2011

22FFL HIGH PERFORMANCE TRANSISTORS



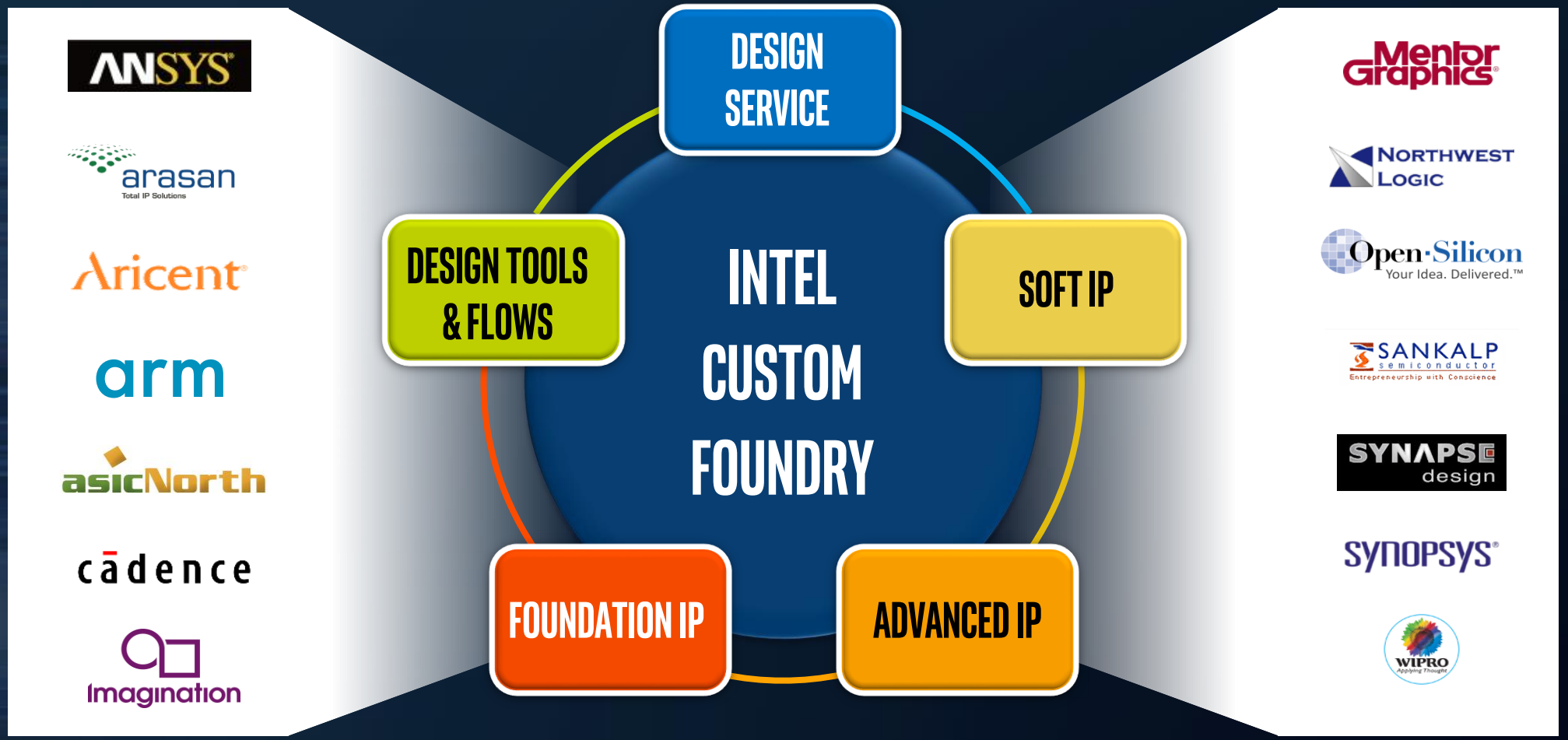
22FFL provides high performance transistors with drive currents similar to 14nm++

22FFL LOW LEAKAGE TRANSISTORS



22FFL provides the lowest leakage transistors for any mainstream technology

INTEL CUSTOM FOUNDRY'S ROBUST ECOSYSTEM

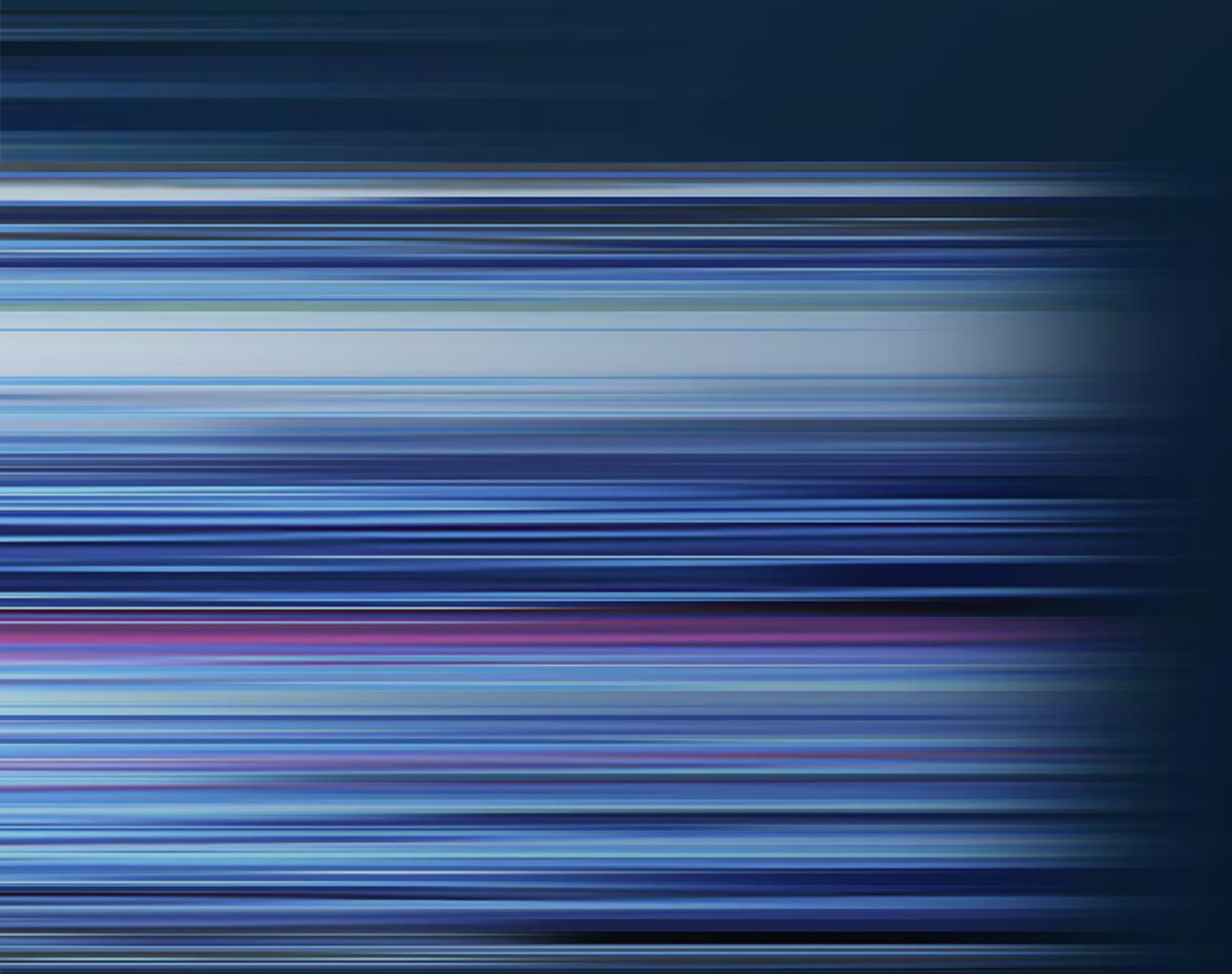


22FFL is fully supported by a robust design ecosystem

22FFL TECHNOLOGY

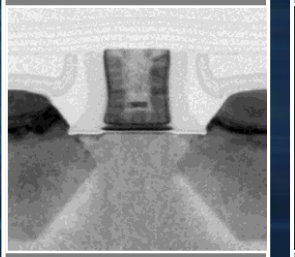
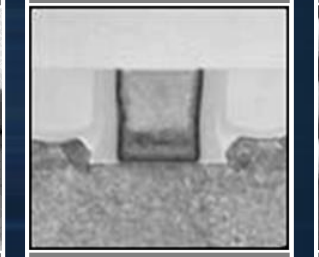
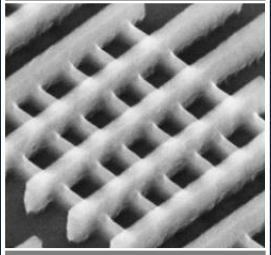
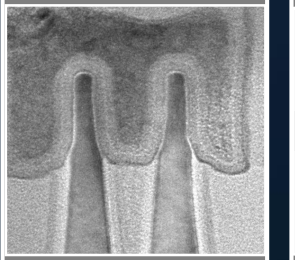
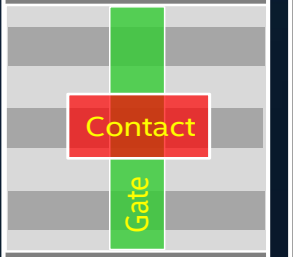
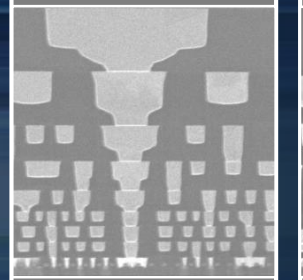
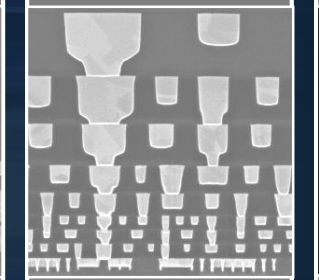
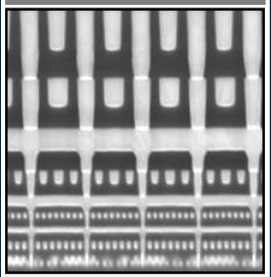
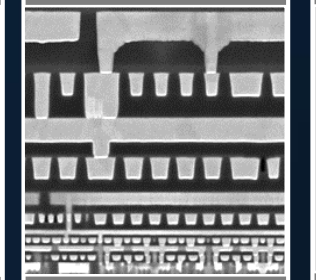
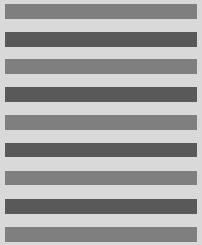
- ✓ High transistor drive currents similar to Intel 14 nm
- ✓ Low leakage transistors with >500x lower total leakage than 22GP
- ✓ Die area scaling better than industry 28/22 nm technologies
- ✓ Wide range of advanced analog/RF devices
- ✓ Extensive use of single patterning for affordable ease-of-design
- ✓ Mature die yield with use of proven 22/14 nm features
- ✓ Cost competitive with other 28/22 nm planar technologies
- ✓ Industry standard PDK1.0 available now
- ✓ Production readiness in Q4 2017

22FFL is an exciting new technology that provides a compelling combination of performance, power, density and ease-of-design for low power IOT and mobile products



10 NM HYPER SCALING
22FFL TECHNOLOGY
FUTURE RESEARCH

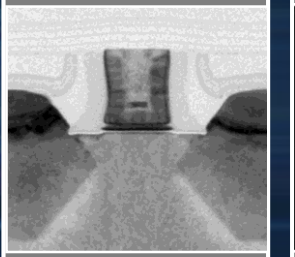
INNOVATION ENABLED TECHNOLOGY PIPELINE

45 nm	32 nm	22 nm	14 nm	10 nm	7 nm	5 nm	3 nm
Manufacturing				Development		Research	
							
High-k Metal Gate		FinFETs		Contact over Gate			
							
			SA Double Patterning	SA Quad Patterning			

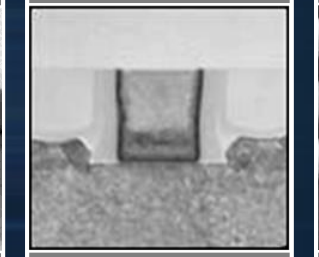
Intel has been the industry leader in bringing innovative technologies from research to high volume manufacturing

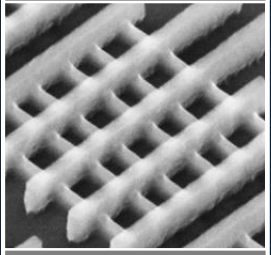
INNOVATION ENABLED TECHNOLOGY PIPELINE

45 nm	32 nm	22 nm	14 nm	10 nm	7 nm	5 nm	3 nm
Manufacturing				Development		Research	

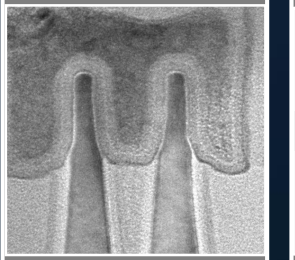


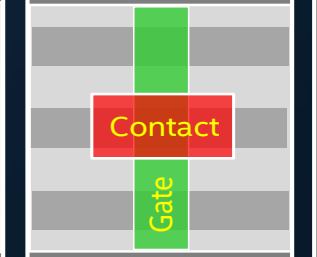
High-k Metal Gate



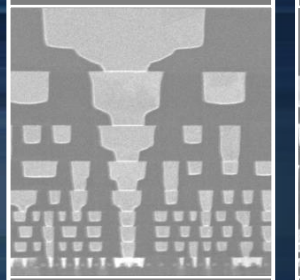


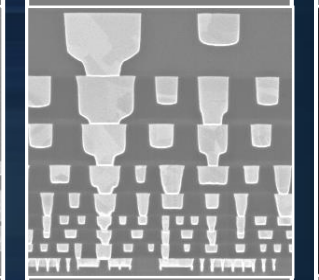
FinFETs

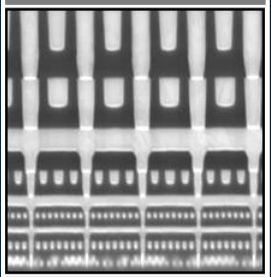


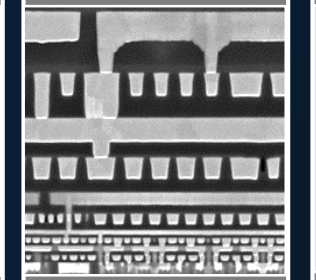


Contact over Gate

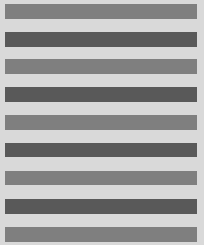




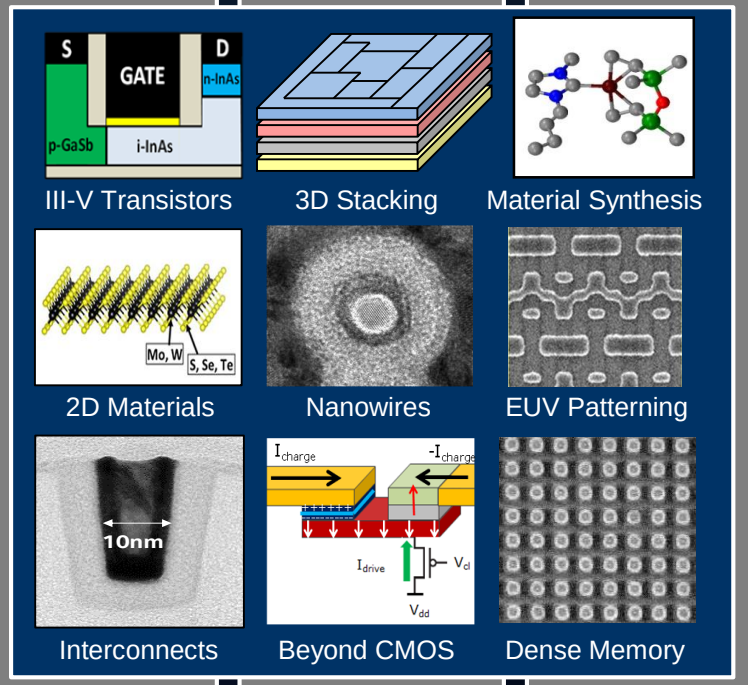




SA Double Patterning



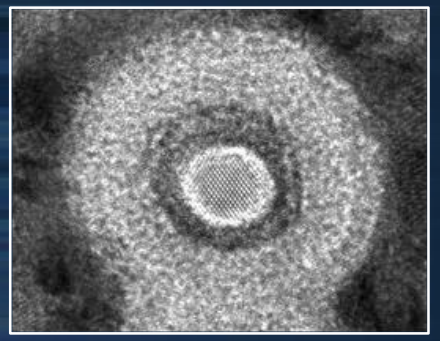
SA Quad Patterning



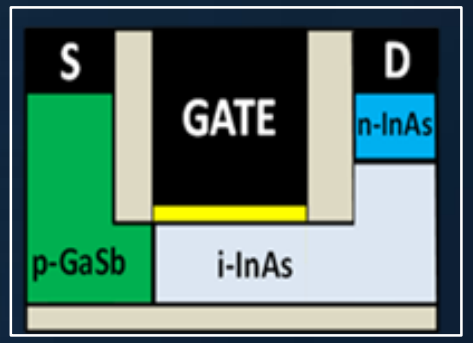
Future options subject to change

We have a wide range of options in research to continue Moore's Law

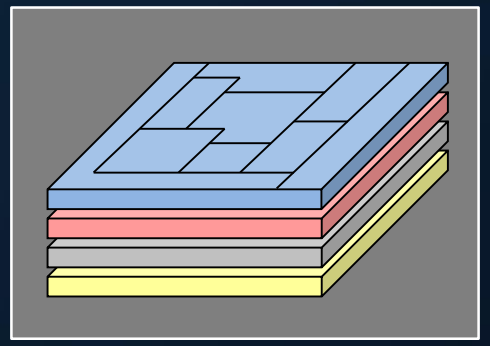
RESEARCH PROJECTS



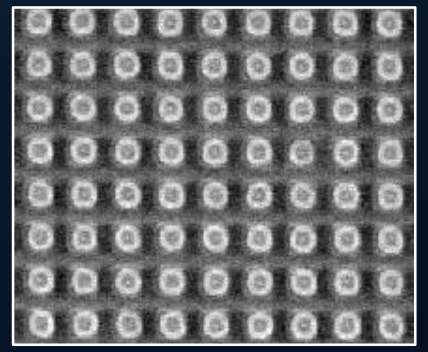
Nanowire Transistors



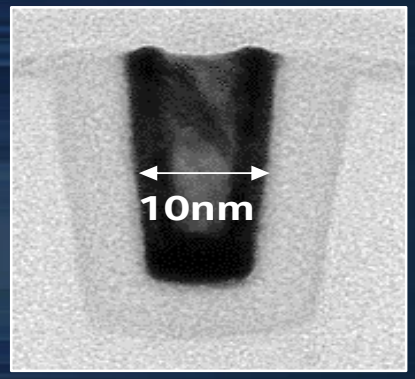
III-V Transistors



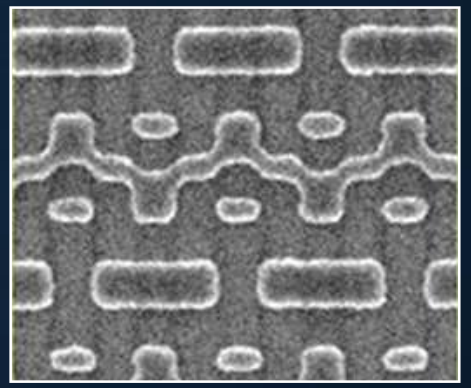
3D Stacking



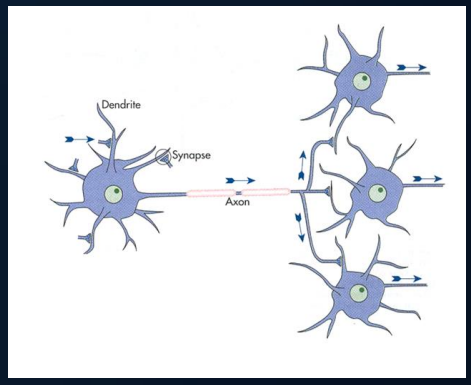
Dense Memory



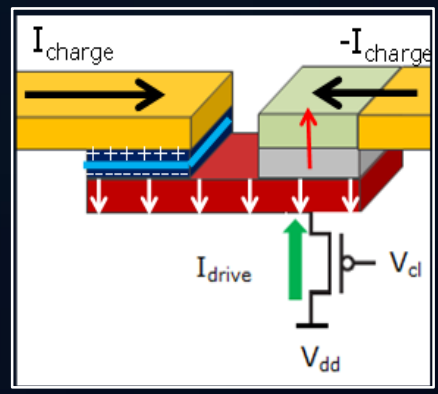
Dense Interconnects



EUV Patterning



Neuromorphic Computing

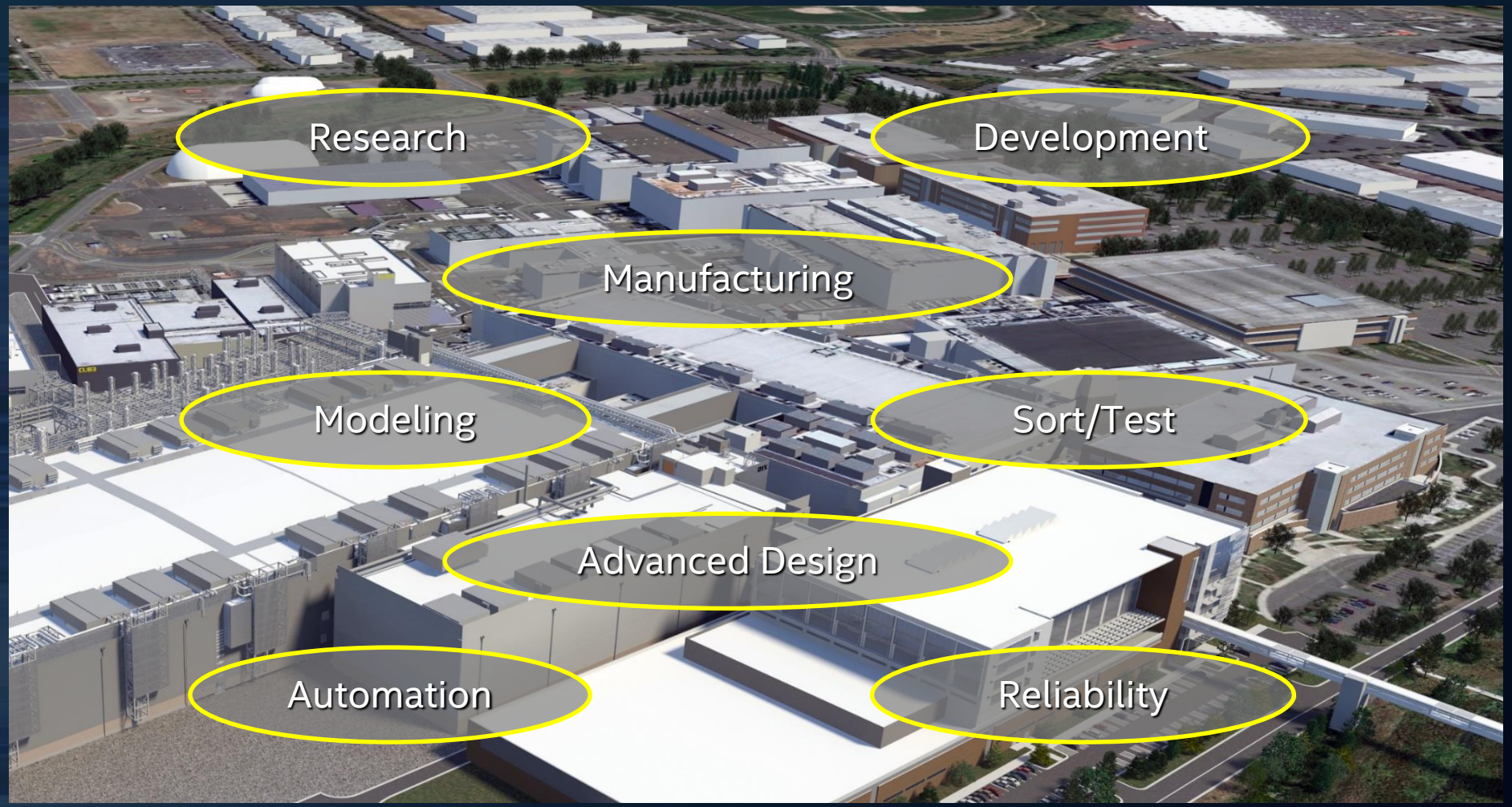


Spintronics

INTEL OREGON CAMPUS

Intel's main research & development site

INTEL OREGON CAMPUS



Technology leadership is the result of close collaboration at one site

SUMMARY

- Hyper scaling on Intel 14 nm and 10 nm technologies provides better than normal scaling and delivers improved cost per transistor and performance per watt
- Intel's 10 nm technology is a full generation ahead of other "10 nm" technologies
- 22FFL provides a compelling combination of performance, power, density and ease-of-design for low power IOT and mobile products
- Multiple technology options now in research will enable the continuation of Moore's Law for at least the next 10 years